REMARKS

Reconsideration of the application in view of the following remarks is requested. Claims 1-14 are in this application. Claims 1 and 11 have been amended. Claims 12-14 have been added to additionally and alternately claim the present invention.

The Examiner rejected claims 1-3, 5-6, and 10-11 under 35 U.S.C. §102(a) as being anticipated by the Admitted Prior Art (APA). The Examiner also rejected claims 4 and 7-9 under 35 U.S.C. §103(a) as being unpatentable over the APA. For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 recites, in part,

> "a semiconductor substrate of a first conductivity type;
> "a well region of a second conductivity type disposed in the semiconductor substrate;
> "a first region of the first conductivity type disposed in the well region on the semiconductor substrate;
> "a second region of the second conductivity type disposed in and on the semiconductor substrate and spaced apart from the first region and the well."

In rejecting the claims, the Examiner pointed to p- substrate 12 shown in applicant's FIG. 1 as constituting the substrate of claim 1, and n-well region 14 as constituting the well region of claim 1. In addition, the Examiner pointed to p+ region 16 shown in applicant's FIG. 1 as constituting the first region of claim 1, and n+ region 18 as constituting the second region of claim 1.

As shown in applicant's FIG. 1, n+ region 18 is not disposed in substrate 12 as required by claim 1, but instead is disposed in n-well 14. The Examiner argues that since n-well 14 is disposed in substrate 12, and n+ region 18 is disposed in n- well region 14, then n+ region 18 is disposed in and on substrate 12.

Applicant disagrees with the Examiner's interpretation. When n-type atoms are introduced into substrate 12, shown in applicant's FIG. 1, n-well 14 is formed and replaces substrate 12. Thus, if n+ region 18 is disposed in well 14, n+ region 18 can not be disposed in substrate 12. However, solely for the purpose of furthering prosecution, applicant has

amended claim 1 to recite that the second region is spaced apart from the first region and the well. Since n+ region 18 of the APA is disposed in n-well 14, it is not possible for n+ region 18 to also be spaced apart from n-well 14.

As a result, claim 1 is not anticipated by the APA. In addition, since claims 2-3, 5-6, and 10 depend either directly or indirectly from claim 1, claims 2-3, 5-6, and 10 are not anticipated by the APA for the same reasons. Further, claim 11 recites "spaced apart from the P+ first region and the N- well," while new claim 12 recites the "spaced apart from the first region and the well" phrase. As a result, claims 11 and 12 are not anticipated by the APA. In addition, since claims 13-14 depend either directly or indirectly from claim 12, these claims are not anticipated by the APA for the same reasons.

With respect to claims 4 and 7-9, the Examiner argued that the APA teaches substantially the entire claimed structure, except the dopant concentrations. However, as noted above, the APA does not teach or suggest an n+ region that is formed in the substrate and spaced apart from both the first region and the well. As a result, claims 4 and 7 -9 are patentable over the APA.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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Dated: 4-1-02 By: _____

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APPENDIX

In the Claims

Please amend the claims as follows:

1. (Amended) An ESD protection structure for an integrated circuit comprising:

a semiconductor substrate of a first conductivity type;

a well region of a second conductivity type disposed in the semiconductor substrate;

a first region of the first conductivity type disposed in the well region on the semiconductor substrate;

a second region of the second conductivity type disposed in and on the semiconductor substrate and spaced apart from the first region and the well; and

an electrical isolation region disposed in the semiconductor substrate between the first region and the second region.

11. (Amended) An ESD protection structure for use with RF frequency integrated circuits comprising:

a P- epitaxial silicon semiconductor substrate;

an N- well region disposed in the semiconductor substrate;

a P+ first region disposed in the N- well region on the P- epitaxial silicon semiconductor substrate;

an N+ second region disposed in and on the P- epitaxial silicon semiconductor substrate and spaced apart from the P+ first region and the N- well; and

an electrical isolation region disposed in the P- epitaxial silicon semiconductor substrate between the P+ first region and the N+ second region.

Claims 12-14 have been added.